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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,764	11/25/2003	Masashi Yonemaru	829-618	3114

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,764	YONEMARU, MASASHI	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-24* is/are pending in the application.

4a) Of the above claim(s) *2,3,5,7 and 9-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,6,8 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 07/05/2005 has been entered.

Specification

2. The title of the invention is not descriptive. A new title is required, such as "INVERTER OR FLIP-FLOP HAVING TWO PMOS IN SERIES AS WELL AS TWO NMOS IN SERIES," that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,6,8, AND 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taki (6,329,845) in view of YONEMARU (2002/0070409).

Taki discloses a semiconductor integrated circuit, comprising a first cell 2 (the first cell 2 is most easily identified in figure 50) comprising a plurality of transistors including a PMOS transistor (the upper of the two transistors in cell 2, as seen in figure 50) and an NMOS transistor (the lower of the two transistors in cell 2, as seen in figure 50); a

second cell 1 (the second cell 1 is most easily identified in figure 50) comprising a PMOS transistor section, the PMOS transistor section comprising a first PMOS transistor (the first PMOS transistor is most easily seen in figure 50, as the uppermost of the four transistors on the left hand side of cell 2. Its source is connected to first source voltage Vdd, and its gate is connected to input signal A, in figure 50) and a second PMOS transistor (the second PMOS transistor is most easily seen in figure 50, as the second uppermost of the four transistors on the left hand side of cell 2. Its source is connected to the drain of the first PMOS transistor, and its gate is connected to first gate control signal D, in figure 50), each comprising a gate, a source, and a drain (note figure 47A) the first and second PMOS transistors being connected in series; and an NMOS transistor section, the NMOS transistor section comprising a first NMOS transistor (the first NMOS transistor is most easily seen in figure 50, as the lowermost of the four transistors on the left hand side of cell 2. Its source is connected to second source voltage GND, and its gate is connected to input signal A, in figure 50) and a second NMOS transistor (the second NMOS transistor is most easily seen in figure 50, as the second lowermost of the four transistors on the left hand side of cell 2. Its source is connected to the drain of the first NMOS transistor, and its gate is connected to second gate control signal B, in figure 50), each comprising a gate, a source, and a drain (note figure 47A), the first and second NMOS transistors being connected in series.

Taki further discloses that a predetermined scheme is used to connect between the first cell 2 and the second cell 1, between the plurality of transistors in the first cell 2, and between the PMOS transistor section and the NMOS transistor sections in second cell 1, that first cell 2 functions as a logic operation circuit (logical "NOT," note figure 49B) for outputting data, that a first source voltage Vdd (note figure 50) is applied to the source of the first PMOS transistor, a second source voltage GND (note figure 50) is applied to the source of the first NMOS transistor, that one of the gate of the first PMOS transistor and the gate of the second PMOS transistor, namely, the gate of the first PMOS transistor, is connected to an input terminal (input terminal "A," seen in figure 47A), the other, namely, the gate of the second PMOS transistor, is connected to a first gate control signal input terminal (input terminal "D," seen in figure 47A), a first gate control signal (first gate control signal D, note figure 50) being input to the first gate control signal input terminal "D," one of the gate of the first NMOS transistor and the gate of the second NMOS transistor, namely, the gate of the first NMOS transistor, is connected to input terminal "A," and the other, namely, the gate of the second NMOS transistor, is connected to a second gate control signal input terminal (input terminal "B," seen in figure 47A), a second gate control signal (second gate control signal B, note figure 50) being input to the second gate control signal input terminal "B," and (note, figure 50, that the drains of the second PMOS and second NMOS transistors are connected together) the drain of the second PMOS transistor and the drain of the second NMOS transistor are connected (via first cell 2) to output terminal Y (again,

please note figure 50). Note figures 47A-B, 48A-B, 49A-B, and 50, and column 14 lines 48-67 of Taki.

Taki does not disclose that the second cell functions as at least one of a driver circuit for driving the logic operation circuit or (specifically with respect to claim 24) as a data retaining circuit for retaining data output by the logic operation circuit.

However, Yonemaru discloses a semiconductor integrated circuit, comprising among other parts a second cell FF1 functioning, through the use of inverter logic circuits I11 through I14, as a data retaining circuit for retaining data output. Note figures 4A, 1B, 1C, and paragraphs 0081, 0083 and 0085 of Yonemaru. Note (paragraphs 0067 and paragraph 0092, figures 1B and 1C) that each of Yonemaru's inverter logic circuits I11-I14 includes either a serial homogeneous PMOS (first and second PMOS transistors being connected in series) or a serial homogeneous NMOS (first and second NMOS transistors being connected in series) circuit identical to the serial homogeneous PMOS and NMOS circuits found in the disclosure of Taki. Therefore, it would have been obvious to a person having skill in the art to replace the second cell of Taki's semiconductor integrated circuit with the second cell functioning as a data retaining circuit for retaining data such as taught by Yonemaru in order to retain data until such time as it is appropriate to output it to thus provide a more flexible data output device.

Response to Arguments

4. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLD
07/05

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